H. N. NAVEEN

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Career Summary

- Master of Technology in Industrial Electronics.
- 16+ years of Hardware, System Design and Product Development experience
- Contributed towards company strategic initiatives and R&D
- Hands-on design and development of Complex high speed, multi-layer product and bring-up boards, Reference boards, Silicon characterization, Product Tear Down analysis, Post-Silicon validation, Handheld product development, GSM handsets, Industrial IoT Gateway, IoT sensor nodes, Medical Devices, Geo-technical measurement products
- Writing Device Datasheets, Board/Product documentation - User manuals, product briefs
- Designed SerDes test boards operating at 28 Gbps per lane
- Multimedia (Tablet PC) product development
- Interact with component vendors, layout, fabrication and assembly houses
- Interface with Industrial Design and Mechanical designers for product design
- Received Achiever of Quarter, Team of Quarter awards for the various projects worked
- Member of IoT4SCTF – IoT for Smart City Task Force, an independent body working on standardizing IoT for smart city applications in India
- Interested in product/system design, research and development

Key Skills

Hardware Tools	:	VNA, Thermonics T-2500, TPO4100, CMU200, In-Circuit Emulators, Synopsys Hardware Modeler, Programmers/debuggers.
Software Tools	:	Schematic Capture (Orcad), Gerber Validation (GC-PREVUE, Viewmate), HDL Simulation (VCS), SI/PI (Hyperlynx)
Microcontrollers/ Processors	:	Freescale i.MX, TI AMxx, Cypress PSoC, Microchip PIC24FJ, PIC32MX, ADI DSP, TI DSP, Intel Silverbutte
Interfaces worked	:	DDR2, DDR3, DDR4, PCI, PCIe 3.0, SATA III, HMC, Video, USB-OTG, USB 2.0/3.0, eMMC, SDIO, NOR, NAND, I2C, I2S.
Soft Skills	:	Passionate towards electronics, Innovative and creative, systematic approach, Possess excellent analytical and communication skills.

Professional Experience

Engineering Manager at **Open-Silicon Research Pvt, Ltd, Bangalore** **since Sep 2011**

- System level architecting
  - Interface with Front-end, Physical Design, Packaging, Software teams for deriving system level architecture
  - Interface with customers for capturing requirements and providing system level solution
- Supporting sales teams during technical discussions with potential customers
- Managing and designing systems
  - Deriving Specifications, Feature lists, component selection, schematic entry, PCB placement and routing validation, BOM creation, SI/PI Analysis, Interaction with PCB fabrication, PCB assembly, Component vendors and Software development group.
  - Signal identification and package ball assignment
  - Writing device datasheets, hardware manuals and user guides.
- Post-silicon validation
  - Validation strategy planning, implementation, interface vs tool identification and procurement.
  - Interaction with front-end, software and driver development teams
- Working on next generation ASIC and SOCs which include

- HBM, HMC, ARM A15, PCIe 3.0, SATA III, 10GBase-KR, USB 3.0, Interlaken (40G+), DDR3, DDR4, HDMI 2.0, IC 2.5D, 3D technology
- Systems worked on
  - Open-silicon IoT edge and gateway platforms, HBM validation board, HMC validation board, 28Gbps Serdes Validation board, FPGA platform daughter cards, 2.5D Validation board

Manager at **ASRT Pvt, Ltd, Bangalore** **Jun 2010 to Aug 2011**

- Design and development of state-of-the art Tablet PC
- Responsibilities include
  - Electrical - Deriving product specifications, Feature lists, Component selection, Schematic entry, PCB placement and routing validation, BOM creation, SI Analysis, Interaction with PCB fabrication, PCB assembly, and Component vendors.
  - Mechanical - Interaction with Industrial design and Mechanical engineers, SLA prototype, Silicon mold vendors.
  - Bring-up/Software - Board bring-up, resolving issues, interaction with software teams, providing inputs for testing.
  - Documentation - Creating process documents, hardware manuals and user guides.
  - Interfaces – 10.1" LCD, DDR2, DDR3, 3G, GPS, GSM, WiFi-BT-FM, LVDS, HDMI, CVBS,USB-OTG, NANDF, eMMC, LAN, UART, SPI, SD Card, SDIO, miniPCIe, I2C and I2S.
  - Management – Project scheduling, project tracking, vendor selection and coordination, releasing purchase orders, payment to vendors,

Lead Engineer at **Sasken Communication Technologies, Bangalore** **Sep 2007 to Jun 2010**

- Design of complex, multi-layer multimedia processor (PNX1005) bring-up and PCI based production board.
- Involved in hardware design, board bring-up, board validation and silicon characterization.
- End-to-end board/product design from defining board specification to production, supporting software teams/customers and documentation
- Designed innovative adapter to validate the new board with previous silicon.
- Create hardware training material for sales and marketing groups

Sr. Design Engineer at **Sasken Communication Technologies, Bangalore** **Feb 2007 to Sep 2007**

- Tear-down Analysis of electronic gadgets

Sr. Design Engineer at **Quasar Innovations Pvt. Ltd., Bangalore** **Dec 2005 to Feb 2007**

- Design of Ultra Low Cost (ULC) GSM handsets.

Sr. Design Engineer at **Sasken Communication Technologies, Bangalore** **Jan 2001 to Dec 2005**

- Develop Hardware Models for complex ASICs and Verification of Synopsys DesignWare IP.

Design Engineer at **Infotech Innovation Research Lab (IIRL), Bangalore** **Jun 2000 to Dec 2000**

- Worked on MPEG1 Layer 3 algorithm

Project Trainee at **Analog Devices India Pvt, Ltd, Bangalore** **Jun 1999 to Jun 2000**

- Designed hardware for Differential GPS receiver (DGPS).

Education

Qualification:

- ***Master of Technology (M. Tech)*** *in* ***Industrial Electronics***
  Institution - Sri Jayachamarajendra College of Engineering (SJCE), Mysore
  University - VTU, Belgaum, 1998 – 2000, Grade – First Class with Distinction, ***University 2nd Rank***

- ***Bachelor of Engineering (B. E)*** *in* ***Electronics and Communication (E&C)***
  Institution - Sri Jayachamarajendra College of Engineering (SJCE), Mysore
  University - University of Mysore, 1993 – 1997, Grade – First Class

Additional Qualification:

- ***Certificate in Machine Learning from Stanford University on Coursera, Apr 2017***

- ***Post-Graduation Diploma*** *in* ***Human Resource Management***
  Karnataka State Open University (KSOU), Mysore, 2000

Awards and Achievements

- Team member - Team of Quarter (TOQ – Q2-12) award for SMC project, Open-Silicon.
- Achiever of Quarter – Technology (AOQ – Q3-09) award for board design and chip characterization, Sasken.
- Team member - Team of Quarter (TOQ - Q2-08) award for Missouri project, Sasken.
- Team member - Team of Quarter (TOQ - Q3-07) award for Telserra Project, Sasken.
- University 2nd Rank, M. Tech Examinations, VTU - 2000.
- Rajiv Gandhi Award-98, given by Rajiv Gandhi Foundation, New Delhi, presented by Mrs. Sonia Gandhi in Aug. 1998.
- 2nd Prize, All India Motorola Discover an Inventor Contest-1999, for developing control system application using MOTOROLA MC68HC705P6A Microcontroller.

Papers and Publications

Publications:

- "*Fully Customizable IoT Gateway SoC Platform Targets Wide Variety of IoT Applications* ", Article published in www.eecatalog.com on 19 Apr'17
- "*Optimized ASIC Design Integrating High Speed SerDes*", Article published in www.chipestimate.com on 14 Feb'17
- "*Validating 2.5D System-In-Package Inter-Die communication on Silicon Interposer*", IEEE EDAPS-2014, Bangalore, IEEE Xplore DOI - 10.1109/EDAPS.2014.7030816.
- Application Note AN2051, "*Precision Digital Controller*", Cypress Microsystems, USA, Nov 2002.
- Application Note AN2xxx, "*Interfacing PS/2 Keyboard using SPI Slave*", Cypress Microsystems, USA, Apr 2005.

Papers/Posters Presented/Submitted:

- "*Optimized ASIC design integrating 28G SerDes*", Poster presented at DAC-2015, San Francisco, USA.
- "*Validating 2.5D System-In-Package Inter-Die communication on Silicon Interposer*", IEEE EDAPS-2014, Bangalore.
- "*A simple, low cost method for re-balling a BGA device*", WACI paper submission, DAC-2009.
- "*BGA PWB: A Simple, Low Cost Method for Testing Complex Embedded Boards*", WACI paper submission, DAC-2009.
- "*Intelligent Transportation: Fleet Management System*", CYBERIA-2000, National level technical event, IEEE, SJCE chapter, Mysore, May 2000.
- "*SSTV: A new approach in High frequency low bandwidth picture transmission*", CYBERIA-98, National level technical event, IEEE, SJCE chapter, Mysore, May 1998.
- "*Advanced Digital Communication Modes in Amateur Radio*", Southern Region Conference of IETE, Mysore, June, 1998.
- "*Multimode Communication Processor for Computing at RF*", CYBERIA-97, National level technical event, IEEE, SJCE chapter Mysore, May 1997.